Variable-Gain Power Amplifier for Mobile WCDMA Applications

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***Abstract*—A single-chip linear power amplifier (PA) with >48-dB gain control range and >24-dBm output power with adjacent channel leakage power below −36 dBc is presented. The chip is realized using an AlGaAs/GaAs heterojunction-bipolar-transistor process and is aimed for 1.95-GHz mobile WCDMA applications. The amplifier consists of two blocks, the variable-gain amplifier, and the PA. The chip size is 1.3 × 1.1 mm^2 and it is mounted on an 8 × 8 mm^2 FR-4 type laminate with 26 pieces of 0402 Surface-mountable discrete components composing a complete 50-Ω input–output amplifier module. This paper presents the design of the two blocks, discusses issues related to their combining, and presents complete amplifier realization and measurement results.**

***Index Terms*—Application-specific integrated circuits, GaAs HBT, gain control, integrated circuit design, linear circuits, microwave integrated circuits, power amplifier.**

I. Introduction

REQUIREMENTS for the RF transmitters needed in new wireless communications systems are again more demanding. The requirement for the dynamic range of the transmission in a general scattering matrix (GSM) system is 28 dB (30 dB in the upper band), whereas in the new WCDMA system, it is 65 dB. This, together with the modulation method requiring linear transmitter parts, forces a new approach be taken for the transmitter architecture.

The requirement of a larger transmission power control range leads to additional transmitter complexity through a separate gain control circuit. The transmission dynamics in the GSM is typically realized by adjusting the bias of the power amplifier (PA). A similar approach is not applicable in systems that require linear transmitter operation since the bias affects strongly the linearity of the PA. A separate gain control block is needed. It has to be linear enough and provide the whole 65 dB of control range in all operation conditions. The practical realizations typically lead to two separate variable-gain amplifiers (VGAs), of which one is a separate integrated circuit (IC) and the other is typically integrated into the transmitter IC containing the other blocks, except the PA. Since the whole 65 dB of gain control cannot be realized with only one IC, a variable-gain PA seems to be the only choice to reduce the transmitter complexity. In this paper, a PA chip that includes a linear-temperature-compensated VGA is presented. This approach reduces the transmitter complexity through reducing the number of required ICs. Size and cost savings are also significant.

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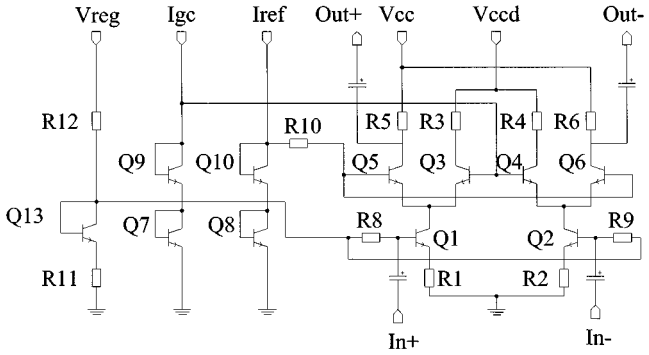


Fig. 1. Schematic of the VGA block and its bias circuits.

The amplifier chip is mounted onto an FR-4-type laminate with 26 pieces of 0402 surface-mountable discrete passive components that are used for matching and filtering. The total size of the amplifier module is 8 × 8 × 1.8 mm^3. The input is balanced and the output is unbalanced; both matched to 50 Ω. The balun performing the differential-to-single-ended transformation is realized on the laminate with four discrete components.

II. VGA Block

The VGA block utilizes the classical Gilbert quad topology. The topology is fully differential and the gain control method is current steering. Various authors have published a number of papers where this same topology has been used successfully [1], [2].

A. Design of the VGA

1) Topology: The schematic of the VGA is shown in Fig. 1. A current steering Gilbert quad topology was chosen for its potential for large gain control dynamics [1]. Due to the relatively low supply voltage requirement of 3.5 V, the current sinking transistors between the emitters nodes of the input transistors ($Q1$ and $Q2$ in Fig. 1) and ground nodes had to be replaced with two separate resistors ($R1$ and $R2$). Better balance between the positive and negative branches could be achieved if the currents from both of the branches would be drawn by the same current sink. Since the relative accuracy of the NiCr resistors in the used process is quite good, a good enough balance could be achieved by using separate resistors. These resistors also provide feedback for the first stage and, thus, improve the linearity and degrade the gain.

2) Sizing the Amplifier: The emitter resistor values in the first stage were chosen to be 30 Ω. According to simulations,

smaller value would result to too a large gain and too low a linearity.

The optimal maximum gain for the VGA block was found to be approximately 6 dB, which is much less than could be achieved with this topology. The total maximum gain of the complete variable-gain PA must not be too high in order not to result to suboptimal performance of the preceding stage of the transmitter.

The output power requirement specification from the VGA was shown to be quite critical. The PA block needed approximately 0 dBm of input power in order to achieve the output power specification of 24 dBm. The size of the load resistors ($R5$ and $R6$) in the common base connected second stage ($Q5$ and $Q6$) was chosen so that, at maximum gain, the output power capability would also be at its maximum. The gain is at its maximum, as all of the bias current is directed through the load resistors and actual amplifying transistors $Q5$ and $Q6$ of the second stage. The dummy current steeling transistors $Q3$ and $Q4$ in this case are completely shut down. The bias current was set to approximately 13 mA in total, 6.5 mA per branch. The knee voltage (V_{Knee}) for the used transistor type is approximately 0.4 V and, therefore, the maximum peak-to-peak voltage swing at the output node is

$$V_{\mathrm{Out},pp} = Vcc - 2V_{\mathrm{Knee}} - I_{\mathrm{Branch}}R_e \tag{1}$$

where the R_e is the emitter resistance value ($R1$ and $R2$), here, 30 Ω, and I_{Branch} is the current flowing through one branch, here 6.5 mA. The resulting available voltage swing value is 2.5 V and the resistor value is chosen so that the voltage drop across it is one-half of the available swing value. 1.25-V drop with 6.5-mA current results to the resistor value of 192 and 200 Ω was chosen for processing reasons.

3) Bias Circuits and Temperature Compensation: The input transistors $Q1$ and $Q2$ are biased with simple current mirror ($Q13$) and a fixed regulated voltage (V_{reg}). The resistor $R11$ needed to be added to the emitter of the current mirror transistor in order to mirror the same base–emitter voltage from the bias circuit to the biased transistors. The size of $R11$ needed to be the same as $R1$ or $R2$. Since the input impedance of the on-biased GaAs heterojunction bipolar transistor (HBT) transistor is sufficiently small, approximately 10-$j30\Omega$ for the unit transistor of this size; two 300-Ω resistors ($R8$ and $R9$) provided sufficient isolation for the bias circuit from the signal. However, 300 Ω is such a small value that the needed base current does not cause notable voltage drop across it and, therefore, the operation of the current mirror is not disturbed.

If the GaAs HBT would be biased with a simple fixed base voltage, the collector current would increase enormously with temperature. This is due to the fact that the base–emitter turn-on voltage of the transistor decreases with rising temperature. This is illustrated in Fig. 2. As the base–emitter voltage is fixed (case 2), the collector current rises from 300 μA to 7.5 mA. The gain, on the contrary, if biased with the fixed collector current (case 1), drops with temperature. A correct biasing, therefore, must be done in such a way that the collector current is increased only slightly with temperature in order to compensate the gain drop (case 2). This can be accomplished by lowering

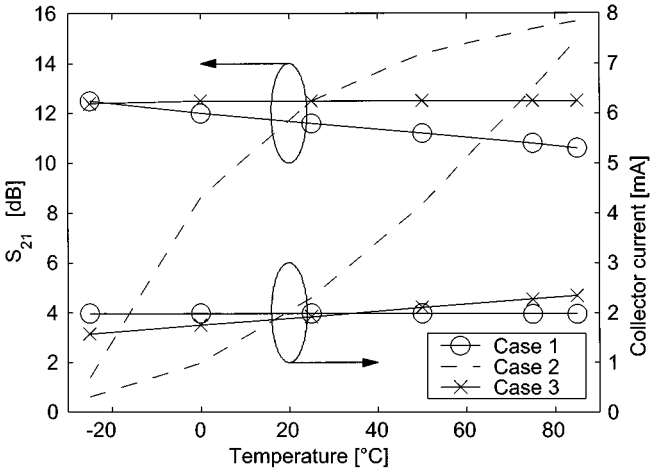


Fig. 2. Simulated $S21$ of the transistor as a function of temperature and the corresponding collector current behavior.

the base–emitter voltage with increasing temperature, but not as much as is inherent to the transistor.

The current mirror bias circuit together with a sufficiently large emitter resistor provides quite good temperature compensation for the gain characteristics of the first stage. The resistor $R12$ also contributes to the temperature compensation since, as more current attempts to draw through it, the bigger the voltage drop across it is and the collector current is prevented from rising.

Since the second stage is cascaded with the first stage, they also share the same collector current. Thus, the collector current of the first stage defines the collector current of the actual amplifying and dummy transistor pairs $Q5$ and $Q3$, and $Q4$ and $Q6$. Despite the bias, current is mainly defined by the first stage, suitable base voltages and currents must be supplied for the second stage in order to bias the transistors on. This is done with two cascaded diode connected transistors pairs $Q10$–$Q8$ and $Q9$–$Q7$ and two external current feeds. By forcing a constant current through the GaAs HBT, its base–emitter voltage will decrease as the temperature increases. By carefully selecting the transistor sizes correctly, a suitably decreasing voltage for the bases of the second stage can be generated; thus, the gain of the stage is constant in different temperatures.

4) Gain Controlling: The gain of the VGA is controlled with two externally generated currents. The currents are fed through the temperature compensations network, as described in the above. The voltage produced by the gain control current (I_{gc}) is fed to the node that connects the bases of the dummy transistors. By setting the current to a very small value ($<$10 μA), the dummy transistors are closed and all the bias current goes through the output transistors; thus, the gain is high. Similarly, by setting the current to a large value ($>$4 mA), the dummy transistor steals all the bias current and the output transistors are closed; thus, the gain of the amplifier is low.

The reference current (I_{ref}) is used to generate a suitable reference voltage to the bases of the output transistors. Its value is kept constant in all conditions. A suitable value was found to be 300 μA. If the reference current would be smaller than 300 μA, the steepness of the gain control curve would increase, i.e., the minimum gain could be reached with a smaller amount

of the control current. The total amount of the needed control currents is critical for the efficiency of the whole transmitter. Small values are desirable in order to save battery lifetime and the size of the controlling chip. The 300-μA reference current value was selected because smaller values would result in too low a voltage level at the $I_{\rm ref}$ node to uphold the two cascaded amplifying transistors ($Q5$ and $Q1$, or $Q6$ and $Q2$) open at high temperatures and low $I_{\rm gc}$ levels. Both simulations and measurements prove that lower $I_{\rm ref}$ values result to a gain collapse, as the $I_{\rm gc}$ is small and the temperature is high.

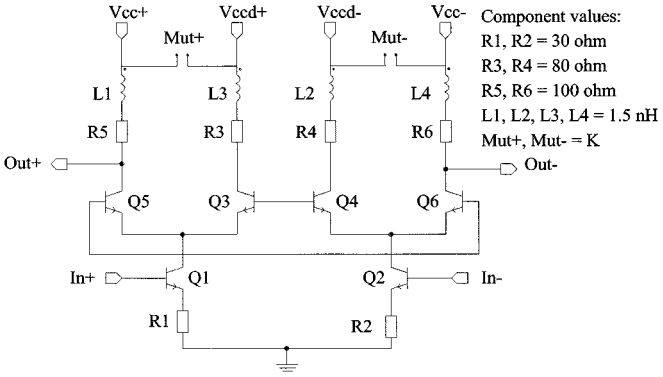
5) Layout and Packaging Issues: Special care was taken for the layout design and package modeling of the VGA. The chip was not actually packaged into a separate package, but the die was mounted straightly on the substrate. In this context, the packaging means the die mounting and wire bonding.

It was found that if there was any coupling between the actual and dummy loads, the gain control dynamics would degrade very fast. As the current is steered from the active transistors to the dummy transistors, the dummy transistors begin to amplify. This amplified dummy signal must be isolated from the amplifier output or the actual loads. The magnitude of this isolation defines the maximum attenuation of this amplifier stage.

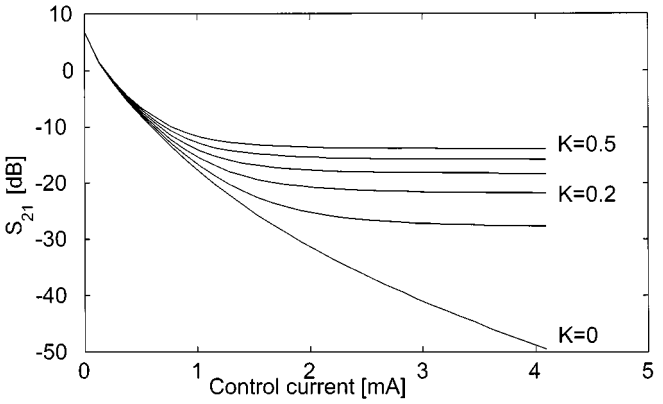
Active and dummy transistors were placed so that on-chip coupling was as small as possible between the critical nodes. Only capacitors of a few tens of femtofarads remain between the nodes due to the necessary metal-to-metal crossings.

A far greater problem was found to be the coupling between the bonding wires. In the very first VGA design, all the supply voltage nodes were separately wire bonded and a model of the bonding wires was implemented to the simulator together with the amplifier circuit. The gain control dynamics degraded from 50 dB to approximately 25 dB after applying the bonding wire model. To verify the source of this problem, a simple test amplifier with a simple bonding wire model was constructed into the simulator. The schematic of the test amplifier is shown in Fig. 3(a). The inductances $L1$–$L4$ represent the series inductance introduced by the bonding wires. The components labeled with "Mut+" and "Mut−" represent the coupling between the bonding wires, and their values are assumed the same. The coupling between bonding wire pairs $L1$, $L3$, and $L2$, $L4$ are ignored for simplicity. The simulated degradation of the gain control dynamics is shown in Fig. 3(b) with different values for the coupling factor K. Roughly, by introducing a 0.2 coupling factor between the bonding wire inductances of the corresponding loads and dummy loads, the maximum attenuation from the amplifier is approximately 20 dB.

In order to minimize the coupling between the actual and dummy loads, virtual ground nodes were formed on-chip. The ground nodes were formed by connecting the supply voltage nodes for the actual loads and dummy loads in different branches together, as is shown in Fig. 1. If there is perfect 180° phase difference between signals in different branches, the formed virtual ground nodes should be ideal signal grounds, and the coupling between the bonding wires does not have any effect on the gain control dynamics. However, any imbalance in balun or signal paths would result in a nonideal virtual ground and degradation of gain control dynamics.



(a)



(b)

Fig. 3. (a) Schematic of the simplified VGA circuit and the bonding wire model. (b) Gain control characteristics of the simplified circuit in different coupling factor values.

To make the amplifier as robust as possible, the supply voltage nodes were bonded from the adjacent corners of the chip. By having a space angle of 90° between bonding wires, the coupling theoretically approaches zero. However, the direction and the shape of the bonding wires is not very accurately controlled because of significant tolerances in die mounting and, therefore, this cannot be used as the sole means to isolate the nodes. Additionally, as big capacitors as possible in the limits of chip dimensions were added between these nodes and the ground node on-chip.

The grounding of the common-base-connected second stage $Q6$ and $Q5$ was also found to be critical. The bases need to have as good a signal ground as possible in order to achieve the largest possible maximum gain. Again, to insure good grounding, the bases of the transistors in different branches were connected together and, initially, the transistors were placed together closely. As in the previous case, the signal grounding is good if the phase difference of the input signal is exact 180°.

The inputs and outputs are dc decoupled with on-chip capacitors that also take part in the impedance matching. The rest of the input matching of the VGA, which is also the input matching of the whole amplifier, is realized with two surface-mountable wire wound inductors on laminate.

B. Measurement Results

The VGA was measured separately in order to define performance bottlenecks for the complete variable-gain PA. The gain

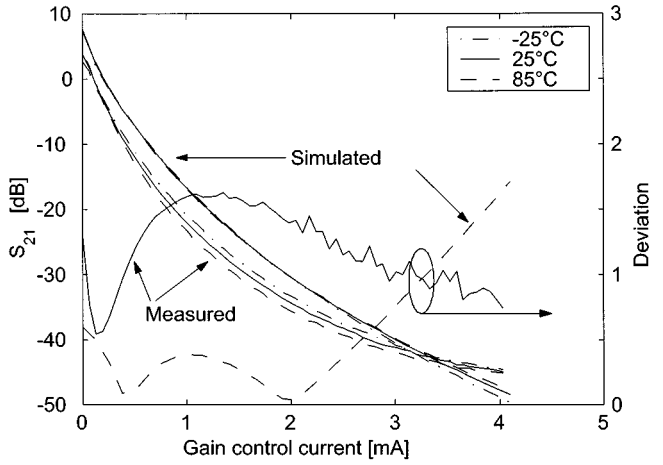


Fig. 4. Gain and maximum deviation of the gain from the nominal curve as a function of the gain control current ($I_{\rm gc}$). Measurement conditions: input power $= -20$ dBm, reference current ($I_{\rm ref}$) $= 300\ \mu$A.

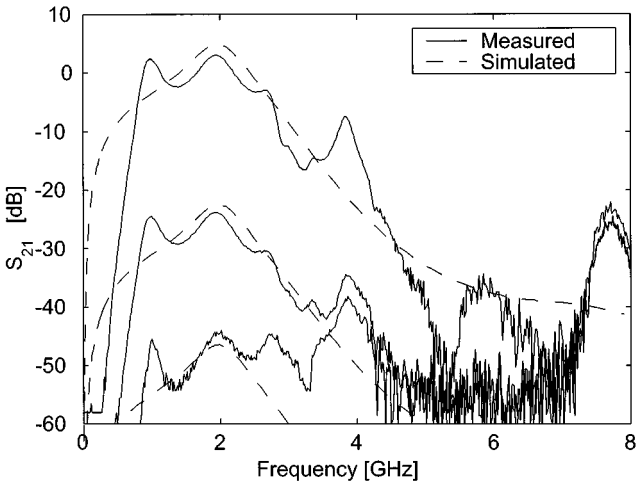


Fig. 5. Magnitude of S_{21} as a function of frequency of the VGA in three different control currents (i.e., 10, 700, and 4096 μA).

control current $I_{\rm gc}$ range was from 1 to 4096 μA and the optimum reference current was found to be 300 μA, as discussed earlier in this paper.

The VGA takes 12 mA from a 3.5-V supply voltage and 5 mA from a 2.7-V regulated voltage. The linearity of the VGA is excellent. The adjacent channel leakage power (ACP) levels are below -40 dBc over all measurement conditions. The maximum input power to the device is -4 dBm and the maximum gain is approximately 4 dB. All the measurements, including the measurements made to the PA block and complete amplifier, are made with a hybrid phase-shift keying (HPSK) modulated signal with a peak-to-average ratio of 3.5 dB.

The measured gain control characteristics are shown in Fig. 4. The deviation curve shows how much the gain varies at a certain $I_{\rm gc}$ value over the whole temperature and frequency range (-25 °C–85 °C and 1920–1980 MHz). The maximum variation is only ± 1.6 dB. The gain curves are measured at a 1950-MHz center frequency. The VGA achieves approximately 48 dB of gain control dynamics throughout the whole temperature range.

The VGA shows potential for very wide-band operation. It preserves the shape of the magnitude curve of the S_{21}, shown in Fig. 5, through all the $I_{\rm gc}$ values over the frequency range from 950 to 2700 MHz. The curve is not flat because the original intention was to tune it to a small frequency range and the commercial baluns used at the input and output have a relative bandwidth of only 10%. However, the gain is equal in the operating 2-GHz band and 1-GHz region, thus, there certainly is potential for at least an octave band operating bandwidth.

III. PA Block

A push–pull topology is utilized in the PA because the VGA in front of the PA is differential. In doing this, we do not need to convert the input signal from differential to single- ended and, therefore, the PA can be placed on the same chip easily. Another thing that inherently supports the use of a differential PA is the fact that it improves the isolation between the VGA input and PA output and, therefore, the gain control dynamics of the VGA will not be degraded. The isolation is improved because there is a virtual ground node at the emitters where the two branches are

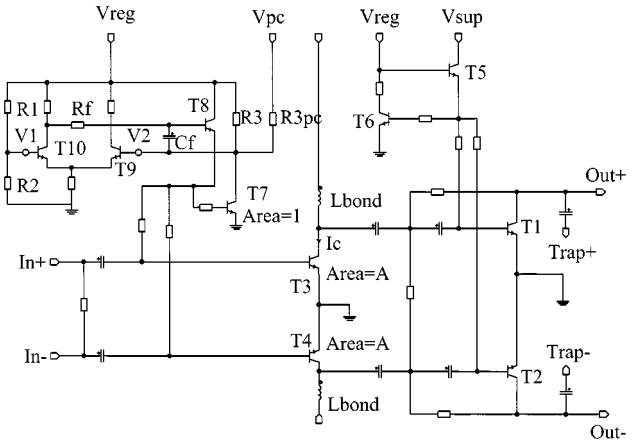


Fig. 6. Schematic diagram of the WCDMA PA chip.

connected together and, at this point, the fundamental and all the other odd harmonic current components cancel each other out [3]. This means that there is no signal component flowing to ground through which it could couple itself back to the input. Fig. 6 presents the schematic diagram of the PA part of the whole chip. All other components presented in this figure are on-chip, except the inductors labeled Lbond. These are part of the interstage matching along with discrete chip inductors on the module. The basic concept is very similar to what we used successfully previously in a GSM PA [3].

A. Realization Issues

This time, only one bias circuit per stage instead of two (as in [3]) was used in order to avoid the possible mismatch in bias currents of the branches that can result from using separate bias circuits. Since dc β of the AlGaAs/GaAs HBT transistor decreases with increasing temperature (i.e., the quiescent current decreases), temperature compensation has to be used when biasing the transistor. A simple way to do this is to employ two diode-connected transistors in series at the base of the current driver transistor (see [5]). This compensation scheme tends to keep the bias current constant as a function of the temperature. Therefore, the gain of the transistor decreases with increasing

temperature, which, in most cases, is not desirable. A more desirable behavior can be achieved by using a bias circuit formed by transistors $T5$ and $T6$ in Fig. 6. This topology is such that when temperature increases, it tends to increase the bias current; thus, compensating the rolloff in dc β of the AlGaAs/GaAs HBT. The $V_{\rm reg}$ node of this bias circuit is connected to the regulated voltage available in a mobile phone [6]. This voltage, however, is not constant, but goes down slightly as the battery voltage drops. A drawback of this bias circuit topology is that it is quite sensitive to the $V_{\rm reg}$ voltage.

To overcome the problems of this bias circuit, a new type of bias circuit based on feedback was proposed [7]. This type of bias circuit is utilized at the driver stage of this WCDMA PA. The core of this bias circuit is similar to the output stage bias circuit. The current driver transistor $T8$ in Fig. 6 feeds the base current for the signal transistors $T3$ and $T4$. Around these, there is a feedback loop, which stabilizes the operating point against temperature, process, and $V_{\rm reg}$ variations. It tends to keep the collector current of the driver constant at all temperatures by increasing the base bias current. Therefore, the gain of the driver will decrease with increasing temperature. The collector current I_c can be calculated using the equation

$$I_c = A*(V_{\rm reg} - V_1)/R_3 + A*(V_{pc} - V_1)/R_{3pc}. \quad (2)$$

In this design, the feedback bias circuit is tuned so that it increases the bias current slightly with temperature compensating some of the gain degradation The voltage V_{pc} in Fig. 6, which is connected to the collector of the current sensing transistor $T7$ through a resistor, can be used for controlling the gain of the driver stage by changing its bias current [6]. It also enables to switch off the power from the driver stage when the PA is not in use. The stability of the control loop is guaranteed by selecting proper values for Rf and Cf in Fig. 6.

Fig. 7 presents measurement results on how the quiescent current changes when the temperature and $V_{\rm reg}$ voltage are varied for the bias circuits of the output stage and the driver stage. It can be seen that, with temperature, the bias circuit of the output stage operates as intended, i.e., it increases the bias current. However, especially at lower $V_{\rm reg}$ values, the current drops considerably, therefore, decreasing the gain of the output stage. The feedback bias circuit also operates as intended, i.e., the quiescent current decreases only slightly when $V_{\rm reg}$ is decreased and it increases somewhat with increasing temperature. Compared to the behavior of the output stage bias circuit, the feedback bias circuit tends to be much more stable against these variations.

The driver stage operates very close to class A with a quiescent current of 33 mA and the output stage is biased to class AB with a quiescent current of 59 mA both at 25 °C and $V_{\rm reg} = 2.8$ V. The combined gain performance of the two amplifier stages is such that simulations predict less than 1.0-dB gain variation for a temperature range from -25 °C to 85 °C.

Shunt resistors were used between the inputs, both at the output and driver stages. These resistors improve the linearity and stability of the amplifier against possible odd-mode oscillations. Both stages were grounded with via-holes through the chip.

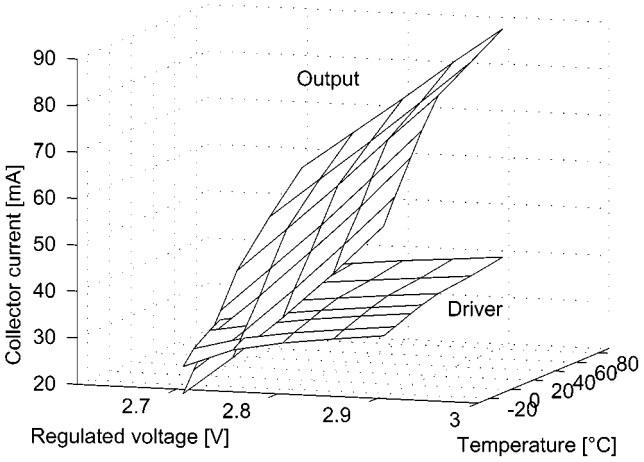


Fig. 7. Measured collector bias current $I_{\rm cc}$ of the output stage and the driver stage as a function of temperature and regulated voltage $V_{\rm reg}$.

B. Measurement Results

The PA was measured separately on a same FR-4 type module as the whole VGA–PA chip. The operating voltage was kept at 3.5 V for all the measurements. The amplifier was found to be stable at all operating conditions and also against load mismatches up to voltage standing-wave ratio (VSWR) 3 : 1. Although the power at the output is combined with a lumped-element *LC–CL* balun [4] so that for one branch, the response is high-pass and for the other, low-pass, the mismatch did not deteriorate the performance of the amplifier considerably. Only small changes could be observed in the measured gain, output power, and ACP values. The output balun also performs the required impedance transformation from 50-Ω single-ended to around 20 Ω per branch at the collectors of the PA output stage. Since there was not the possibility to perform load–pull measurements for the output stage, the optimum impedance level had to be selected based only on simulations. Some load–pull simulations were done, but since there was not a WCDMA signal source available in the simulator, the selection of the impedance level was done based on the output power and efficiency figures. The linearity was checked after the impedance level was fixed and if it did not fulfill the requirements, another value was selected. Coilcraft wire-wound chip inductors and Johanson Technology C-series high-frequency chip capacitors are used in the balun. At the input side, the differential input signal for the PA was generated with a Murata LBD-series monolithic balun.

The efficiency of the PA module with 3.5-V operating voltage was measured to be 36% when the output power was 24 dBm. At this point, the adjacent channel power (i.e., ACP1) was -42 dBc and the next adjacent channel power (i.e., ACP2) was -55 dBc. With a 3.3-V operating voltage, the PA achieved power-added efficiency of 38% and $\mathrm{ACP1} = -38$ dBc, which still fulfills the linearity specification of $\mathrm{ACP1} < -36$ dBc.

IV. Complete Variable-Gain PA

A. Implementation Issues

Finally, the complete VGA was constructed by combining the separately designed VGA and PA blocks on the same chip.

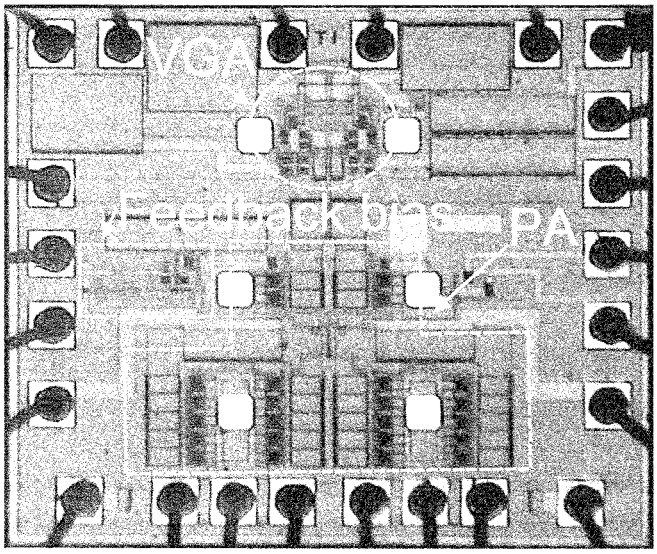
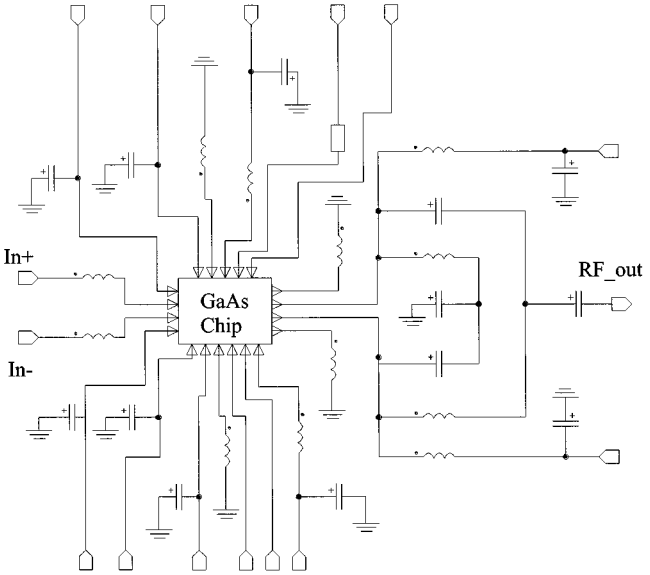
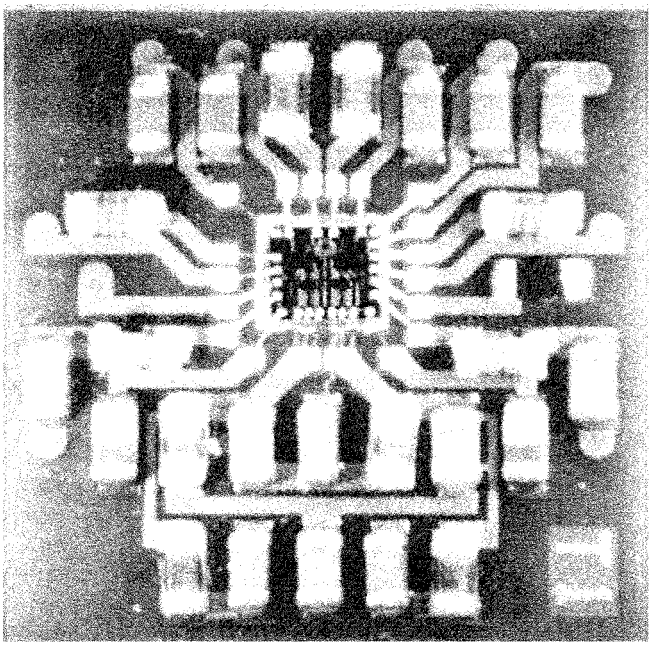


Fig. 8. Variable-gain PA chip.



(a)



(b)

Fig. 9. (a) Schematic. (b) Photograph of the VGA–PA module.

Both blocks are differential, which makes the combining easier. The chip has 19 input/output pins with 23 bond wires that are wire-bonded to the module. Fig. 8 presents a micrograph of the chip having the size of $1325 \times 1105\ \mu\text{m}^2$. The control currents and voltages are the same as for the individual blocks described in the previous chapters.

The schematic of the VGA–PA module is shown in Fig. 9(a) and a photograph of the module is shown in Fig. 9(b). The interfunction matching between the VGA and PA blocks was realized with on-chip series capacitors and off-chip parallel inductors. Seven capacitors are used only as bypass capacitors for control and supply voltage lines and are not necessarily needed.

B. Measurements

The amplifier operated as predicted in the simulations and did not need any tuning in the laboratory. No oscillations were observed during measurements, although the GaAs HBTs and single-chip multistage amplifiers tend to be very prone to instability in general.

The amplifier draws 103-mA dc current from the 3.5-V supply and 14 mA from the regulated voltage without any input signal at the nominal temperature of 25 °C. In addition to the supply and regulated voltages, a reference and gain control current for the VGA block and a fixed Vpc voltage for the PA are needed.

The measured output power at 1.95 GHz as a function of the control current at different temperatures (−25 °C to 85 °C) is shown in Fig. 10. The gain control range of $>$48 dB is achieved in all temperature conditions and the variation of output power at a certain I_{gc} value over all temperatures and frequencies is less than $\pm$2.7 dB and the shape of the curve is nice and smooth. The variation of output power in temperatures at the center frequency of 1950 MHz is less than $\pm$1.8 dB. The required maximum output power of 24 dBm is reached at all temperatures. The gain control range can be further increased by controlling the Vpc voltage at the bias circuit of the first stage of the PA block. In this way, a gain control range of 65 dB was measured without compromising the linearity performance.

The linearity of the amplifier is good, the ACP figures are below −36 dBc in all measurement conditions, and the output power requirement of 24 dBm is fulfilled. The power-added efficiency of the whole amplifier at 24 dBm is $>$27% at minimum and a peak of 39% was measured at 1.92-GHz center frequency and −25 °C ambient temperatures. In that measurement point, the output power was 26 dBm and the linearity requirements were fulfilled. The nominal performance values with 24-dBm output power are 28% and $\text{ACP1} = -41.6$ dBc at 1.95 GHz. The ACP and the power-added efficiency at 1.95 GHz are shown in Fig. 11. The increase in the ACP figures as the output power drops below 0 dBm is due to the measurement setup. The noise

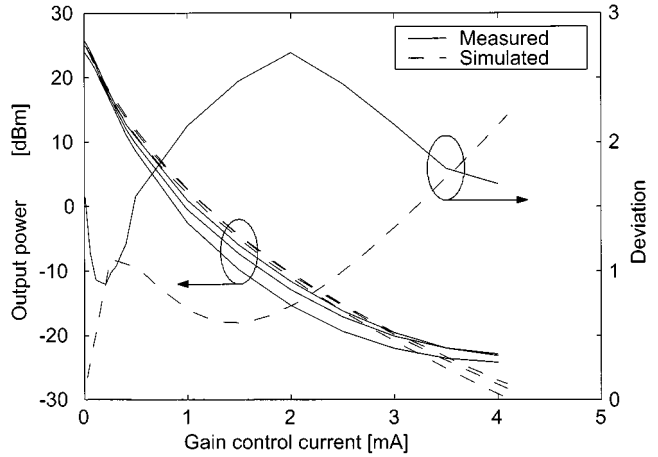


Fig. 10. Output power and the maximum deviation from the nominal output power at 1.95 GHz as a function of control current at three different temperatures (-25 °C, 25 °C, and 85 °C). The input power is kept constant at -9 dBm.

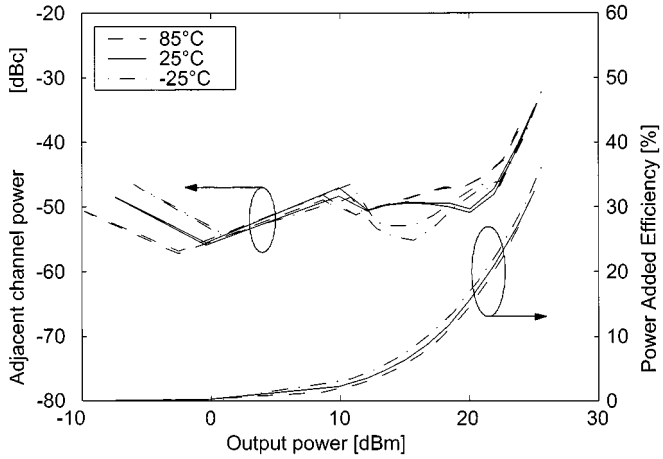


Fig. 11. Measured ACP and power-added efficiency at 1.95 GHz as a function of output power at three different temperatures. The input power is -9 dBm.

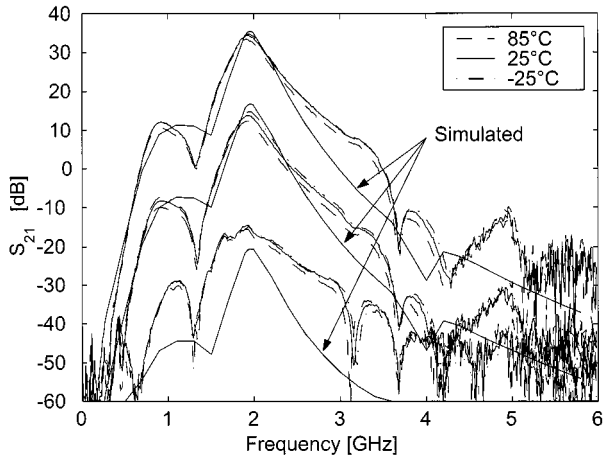


Fig. 12. S_{21} of the amplifier at three different gain control currents (10, 700, and 4096 μA) and at three different temperatures (-25 °C, 25 °C, and 85 °C) as a function of frequency (from 0 to 6 GHz). Measurement source power is -20 dBm.

floor of the analyzer starts to distort the measurement results at low-output power levels.

TABLE I
PERFORMANCE SUMMARY OF THE AMPLIFIER

Parameter	Value	Unit	Comment
Operating frequency	1920 – 1980	MHz	
Supply voltage	3.0 – 5.0	V	
Operating temperature	-25 – 85	°C	
Gain	-14 – 35	dB	-30 to +35 extended range with *Vpc* utilized
Output power	> +24	dBm	
Adjacent channel leakage power	< -36	dBc	
Power added efficiency @ 24 dBm output power	> 27	%	
Peak power added efficiency	39	%	

The scattering parameters were measured over the whole temperature range and at three different I_{gc} values. The shape of the magnitude curve of S_{21} is shown in Fig. 12. The small change in temperatures can be viewed in the middle curve, which corresponds to the $I_{gc} = 700$ μA. The -10-dB bandwidth of the S_{11} is as wide as 288 MHz at all temperature and I_{gc} values, whereas the requirement was only 60 MHz (from 1.92 to 1.98 GHz).

Table I summarizes the performance of the variable-gain PA module. These results, as are all of the results presented in this paper, are measured from an FR-4 test board on which the module was mounted. The results include losses of the input balun and transmission lines on a printed circuit board.

V. CONCLUSIONS

In this paper, a linear variable-gain PA has been realized as a single-chip solution. Accurate temperature compensation has also been realized with a simple circuitry implemented on the same chip as the amplifier. The amplifier has showed a maximum gain variation of ± 2.7 dB over the whole temperature and operation frequency range, an output power 24 dBm with efficiency greater than 27%. A peak efficiency of 39% with the output power 26 dBm has been measured while fulfilling the required -36-dBc ACP figures. The physical size of the 50–50-Ω amplifier module including all the required components is $8 \times 8 \times 1.8$ mm^3 (0.115 cm^3).

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